Miniaturized low-power artificial compound eyes in a small form factor and a low payload can be a promising approach to provide wide-field information for micro-air-vehicle (MAV) applications. Recently, research efforts have been made to realize bio-inspired artificial compound eyes to mimic the wide field of view (FoV) of insect visual organs by implementing photoreceptors to independently face different angles [1-2]. However, these approaches have drawbacks. They use complicated fabrication processes to form a hemispherical lens configuration and secure an independent optical path to each photoreceptor. We take a simple and practical approach to realize wide-field optic flow sensing in a pseudo-hemispherical configuration by mounting a number of 2D array optic flow sensors on a flexible PCB module as shown in Figure 7.2.1. In this scheme, the 2D optic flow sensor should meet the requirements of MAV applications: extremely low power consumption while maintaining robust optic flow generation. Conventional optic flow algorithms, such as Lucas-and-Kanade, require huge amounts of numerical calculations; therefore, they require substantial digital hardware (GPU and/or FPGA), resulting in large power consumption [3-4]. As an alternative approach for low-power implementation, bio-inspired elementary motion detector (EMD) based algorithms (or neuro-photomorphic algorithms) have been studied and implemented in analog VLSI circuits for autonomous navigation [5-6]. However, pure analog signal processing is easily susceptible to temperature and process variations and it is difficult to scale the pixel size or apply low-power design techniques because extensive analog processing is implemented in pixel-level circuits. In this work, we have devised and implemented a time-stamp-based optic flow algorithm, which is modified from the conventional EMD algorithm to give an optimum partitioning of hardware blocks in analog and digital domains as well as assign adequate allocation of pixel-level, column-parallel, and chip-level processing.

Temporal filtering, which may require huge hardware resources if implemented in the digital domain, remains in a pixel-level analog processing unit. Feature detection is implemented using digital circuits that are column parallel. The embedded digital core decodes the 2D time-stamp information into velocity using chip-level processing. Finally, the estimated 16b optic flow data are compressed and transmitted to the host through a 4-wired Serial Peripheral Interface (SPI) bus.

Figure 7.2.1 shows the conceptual view of the semi-hemispherical artificial compound eyes and its system architecture. The system is designed to provide wide-field optic flow sensing, which covers 180° FoV per each module like a compound eye in flying insects. To realize the wide FoV, the system mounts multiple optic flow sensors on a flat flexible PCB; then, the PCB is bent to form the desired inter-sensor angle by origami packaging. The host controller, which may be located at the bottom of the PCB packet, communicates with all the sensors by 4-wired SPI. The 3MB/s SPI, currently the fastest bus available in MAV systems, can only send full resolution (8KB) raw optic flow data at 120fps from 3 sensors. Thus, the sensor integrates the lossless data compression algorithm to reduce the data rate down to 12.0% of the total data on average, so that at least 25 sensors can be connected in the same bus.

Figure 7.2.2 shows the pixel architecture and system block diagram of the bio-inspired time-stamp-based optic flow sensor. In normal image mode, the sensor generates 8b digital images from the embedded single slope (SS) ADCs. In optic flow mode, the sensor operates as a bio-inspired vision chip emulating insect vision by estimating optic flows from the time-of-travel of a moving feature that is detected by temporal contrast changes. First, the temporal contrast change is monitored from two consecutive frames in the pixel array.

The pixel includes a sampling capacitor ($C_1$) and the gain capacitor ($C_2$) for setting a PGA gain. A frame difference is acquired by sampling the pixel voltage ($V_{p}(t)$) of the previous frame from $C_1$ first and then applying the current pixel voltage ($V_{p}(t+1)$) to the PGA. Two supply voltages are used in the pixel array: 3.5V for photodiodes and source followers, and 1.8V for PGAs. To reduce static power consumption, the PGAs are enabled only during the signal transfer period. The column-level digital circuits use a 0.9V supply. A 1b comparator detects the moving feature when there is a significant change in the temporal contrast beyond a threshold that can be dynamically adjusted. The column-parallel 1b feature information enables the embedded 2D optic flow digital core to update recent time-stamp information when a moving feature appears in each pixel. The 1.8V supply digital core estimates 16b raw optic flows, representing 8b for each x and y direction. The generated raw optic flows are compressed and sent to the host.

Figure 7.2.3 shows the block diagram of the embedded digital processing unit in detail. The 2D optic flow computation core first stores in SRAM the time-stamp information of the recent occurrence of a moving feature in each pixel. The updated time-stamp information is aligned to those from the previous ones in a raster scan order to estimate 2D optic flows by a 3×3 masking operation. Two computation examples are illustrated at different times at $t=12$ and 14. At time $t=12$, a vertically moving feature enters to the center with a speed of 1 pixel/frame; the time-stamp value reflects this change. As a result, only the y-direction time-of-travel is measured at the updated location, and the final estimated optic flow is $(V_x, V_y) = (0, 1)$. In the same manner, at time $t=14$, the optic flow of $(V_x, V_y) = (0.5, 0)$ is estimated. The calculated 16b raw optic flows can be compressed in the lossless data compression block. We employ a compression algorithm that utilizes sparsity in signals, which is the nature of typical optic flows. As shown in an example presented in the histogram, the 94.6% of pixels in one frame are at zero (i.e., no optic flows). The compression algorithm sends only a 1b code for zero optic flows and sends a 2b header plus a 1b raw optic flow value (total 18b) for non-zero optic flows. As a result, the algorithm allocates 1.92b on average instead of a uniform allocation of 16b for each pixel, achieving 88% reduction in bandwidth. Because the compressor output is either 1b or 18b depending on optic flow values, the packetizing block piles up the compressed data and outputs 64b packets to be stored in the output buffer SRAM.

Figure 7.2.4 shows the measured performance of the fabricated 2D optic flow sensor. The linearity curve was characterized by averaging the output optic flows while applying the fixed velocity input patterns. (We applied the moving bar patterns for characterization.) The circles show the measured data from the whole sensor signal path. The triangles show only for the digital core by directly loading the input patterns to the core using the test ports. The mismatch between these two results may come from the imperfection of optics and/or non-uniformity in input patterns projected from LCD monitors. We also tested simple computer-generated patterns: translating, diagonally moving, and rotating patterns at 30fps (Fig. 7.2.4). We also successfully captured optic flows in 3 test cases: a fan rotating at 160 rpm, a bouncing ball, letters written by tracking a laser pointer source, demonstrating the performance and feasibility for deploying the fabricated sensor in actual MAV platforms (Fig. 7.2.5).

A prototype chip was fabricated using a 0.18µm 1P4M process. The performance of the sensor is summarized in Fig. 7.2.6. We achieved a figure of merit of 243.3pJ/pixel to estimate 16b 2D optic flows. A chip micrograph is shown in Fig. 7.2.7.

References:
Figure 7.2.1: Artificial compound eyes platform.

Figure 7.2.2: Sensor and pixel architecture.

Figure 7.2.3: Digital-processing blocks (2D optic flow core and compressor).

Figure 7.2.4: Characterized optic flow performance.

Figure 7.2.5: 2D optic flow tests of moving objects.

Figure 7.2.6: Chip characteristics.
Figure 7.2.7: Chip micrograph.